UNITED STATES PATENT APPLICATION

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FOR

METHOD AND APPARATUS FOR DATA-DRIVING ELECTRO-LUMINESCENCE DISPLAY PANEL DEVICE

[0001] The present invention claims the benefit of Korean Patent Application No. P2002-51087 filed in Korea on August 28, 2002, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0002] The present invention relates to a display panel device, and more particularly to a method and apparatus for data-driving an electro-luminescence display panel device.

DESCRIPTION OF THE RELATED ART

[0003] Currently, various flat panel displays are being developed to have reduced weight and overall size to replace cathode ray tube (CRT) devices. These flat panel displays include liquid crystal display (LCD) devices, field emission display (FED) devices, plasma display panel (PDP) devices, and electro-luminescence display (ELD) devices. Accordingly, these flat panel display devices can be classified into voltage drive devices and current drive devices.

[0004] The ELD devices are self-luminous, wherein fluorescent materials emit light by re-combining electrons with holes. The ELD devices have fast response speeds, as compared to CRT devices and passive-type luminous devices that require separate light sources, such as the LCD devices. The ELD devices may be considered current drive-type and voltage drive-type, and can generally be classified into inorganic ELD and organic ELD devices in accordance with their materials and structures.

[0005] FIG. 1 a schematic cross sectional view of an organic electro-luminescence display device according to the related art. In FIG. 1, an organic ELD device includes an electron injection layer 4, an electron transport layer 6, a light emission layer 8, a hole transport layer 10, and a hole injection layer 12 that are deposited between a cathode 2 and an anode 14. If a voltage is supplied between the anode electrode 14 of a transparent electrode material and the cathode electrode 2 of a metal electrode material, electrons generated from the cathode 2 move toward the light emission layer 8 through the electron injection layer 4 and the electron transport layer 6. Furthermore, holes generated from the anode 14 move toward the light emission layer 8 through the hole injection layer 12 and the hole transport layer 10. Accordingly, the electrons and the holes supplied from the electron transport layer 6 and the hole transport layer 10 collide in the light emission layer 8 to re-combine, thereby generating light that is emitted through the anode 14 to an exterior to display an image. A luminous brightness of the ELD device is not proportional to a voltage supplied to both ends of the device, but is proportional to a supply current. Thus, the anode 14 is normally connected to a constant current source.

[0006] FIG. 2 is a schematic plan view of an active matrix-type electro-luminescence display device according to the related art. In FIG. 2, an active matrix-type ELD device includes an ELD panel 16 having a pixel 22 arranged at each intersection part of scan lines SL and data lines DL, a scan driver 18 to drive the scan lines SL, and a data driver 20 to drive the data lines DL. Each of the pixels 22 are selected when scan pulses are supplied

to the scan line SL of a cathode to generate light corresponding to a pixel signal, i.e., a current signal supplied to the data line DL of anode. The pixels 22 include an electro-luminescence (OEL) cell and a cell driver. Each OEL cell may be equivalently expressed as a diode connected between the data line DL and the scan line SL, wherein each OEL cell emits light when a negative scan pulse is supplied to the scan line SL and a positive current is simultaneously supplied to the data line DL in accordance with a data signal, thereby supplying a forward voltage. Alternatively, a reverse voltage is supplied to the OEL cell included in an unselected scan line, whereby no light is emitted. In other words, the light-emitting OEL cell is charged with a forward charge, whereas the OEL cell with no light emission is charged with a reverse charge.

[0007] The scan driver 18 sequentially supplies the negative scan pulse to scan lines SL, and the data driver 20 supplies a current signal to the data lines DL, wherein the current signal has a current level or pulse width corresponding to a data signal for each horizontal period. Accordingly, the ELD device supplies the current signal with the current level or pulse width proportional to input data to the OEL cell, and each OEL cell emits light in proportion to the amount of current applied from the data line DL.

[0008] FIG. 3 is a schematic circuit diagram of a data driver shown in FIG. 2 according to the related art. The data driver 20 controls the pulse width of the current signal in response to the input data, and includes a plurality of data drive integrated circuits (ICs) and a data drive IC 21, which mainly uses a current mirror circuit in order to create a constant current.

[0009] In FIG. 3, the data driver IC 21 includes a reference MOSFET M0 connected between a voltage source VDD and a ground voltage source, wherein the constant current sources, i.e., constant current supply MOSFETs M1 to M4 that are connected to the voltage source VDD and, at the same time, connected in parallel to the reference MOSFET M0, form a current mirror circuit for supplying the constant current (i) to each data line connected to the OEL cell 24. In addition, the data drive IC 21 includes switch devices S1 to S4 that are connected between the constant current supply MOSFET M1 to M4 and the data line to control a supply time of the constant current (i) from the constant supply MOSFET M1 to M4 in response to the input data, thereby controlling the pulse width of the current signal. Accordingly, it is possible for the data drive IC 21 not to include the switch devices S1 to S4.

[0010] Each of the constant current supply MOSFETs M1 to M4 together with the reference MOSFET M0 receive the supply voltage of the voltage source VDD in parallel to form a current mirror circuit with the reference MOSFET M0. Accordingly, the same amount of constant current (i) or 2^n times the constant current, i.e., 2i, 4i, 8i,..., is supplied. The constant current (i) supplied from the constant current supply MOSFETs M1 to M4 changes in accordance with the amount of load, i.e., line resistance, of the data lines and capacitance that are both related to the amount of light emission of the OEL cell 24 due to the structure of the ELD panel. Accordingly, the data drive IC 21 includes a plurality of current control resistors each having resistance values different from each other in order to

control the changing current in accordance with the amount of load. In addition, a resistor is selected among the plurality of current control resistors in accordance with an average amount of load of the data drive IC 21 to be connected between the reference MOSFET M0 and ground, thereby controlling the constant current (i) of the data drive IC 21.

[0011] The data driver 20 includes a plurality of data drive IC's 21, as shown in FIG. 3. In addition, another reference current source to the external voltage source is required for each data drive IC 21 to supply the reference current to the reference MOSFET M0. Accordingly, the output of each reference current source needs to be equal in order to reduce the current output deviation between the data drive IC's 21. Thus, each data drive IC 21 uses the same external voltage source VDD, and each current source needs to be adjusted for equalizing the reference current.

[0012] However, the active matrix-type ELD device has its own problems. For example, when the number of reference current sources increases, more operational time is required to adjust the reference current sources when a plurality of data drive IC's 21 are used.

SUMMARY OF THE INVENTION

[0013] Accordingly, the present invention is directed to a method and apparatus for a data-driving an electro-luminescence display panel device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0014] An object of the present invention is to provide a data-driving apparatus and method of an electro luminescence display panel that reduces output deviations between data drive IC's.

[0015] Another object of the present invention is to provide a data-driving apparatus and method of an electro-luminescence display panel that reduces a control time of a current source from an external voltage source.

[0016] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0017] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a data-driving apparatus of an electro-luminescence display panel includes a display panel receiving a current signal to display an image, and a data driver having a plurality of current sink data drive parts in order to supply data to the display panel based on a constant current, wherein the current sink data drive part comprises a current sink data drive integrated circuit for supplying the data to the display panel based on the constant current, and a reference current supply/path part for supplying the constant current to the current sink data drive integrated circuit and,

at a same time, supplying the same constant current to an adjacent current sink data driver in a cascade circuit configuration.

[0018] In another aspect, a data-driving apparatus of an electro luminescence display panel includes a display panel receiving a current signal to display an image, and a data driver having a plurality of current source data drive parts to supply data to the display panel based on a constant current, wherein the current source data drive part comprises a current source data drive integrated circuit for supplying the data to the display panel based on the constant current, and a reference current supply/path part for supplying the constant current to the current source data drive integrated circuit and, at the same time, supplying the same constant current to an adjacent current source data driver in a cascade circuit configuration.

[0019] In another aspect, a data-driving method of an electro-luminescence display panel having a pixel formed at each intersection part of scan lines and data lines, a scan driver to control the scan lines and a data driver to control the data lines includes steps of simultaneously supplying a constant current generated by an external voltage source to a current sink data integrated circuit and an adjacent current sink data integrated circuit, which are connected in a cascade circuit configuration within the data driver, and supplying data to the data lines based on the supplied constant current.

[0020] In another aspect, a data-driving method of an electro-luminescence display panel having a pixel formed at each intersection part of scan lines and data lines, a scan driver to control the scan lines and a data driver to control the data lines includes steps of

simultaneously supplying a constant current generated by an external voltage source to a current source data integrated circuit and an adjacent current source data integrated circuit, which are connected in a cascade circuit configuration within the data driver, and supplying data to the data lines based on the applied constant current.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0022] FIG. 1 is a schematic cross sectional view of an organic electro-luminescence display device according to the related art;

[0023] FIG. 2 is a schematic plan view of an active matrix-type electro-luminescence display device according to the related art;

[0024] FIG. 3 is a schematic circuit diagram of a data driver shown in FIG. 2 according to the related art;

[0025] FIG. 4 is a schematic circuit diagram of an exemplary active matrix-type electro-luminescence display apparatus according to the present invention;

[0026] FIG. 5 is a schematic circuit diagram of an exemplary cell of an electro-luminescence display panel of FIG. 4 according to the present invention;

[0027] FIG. 6 is a schematic diagram of an exemplary configuration of a data driver according to the present invention;

[0028] FIG. 7 is a schematic diagram of an exemplary current sink data drive IC part of FIG. 6 according to the present invention;

[0029] FIG. 8 is a schematic circuit diagram of the current sink data drive IC part of FIG. 6 according to the present invention;

[0030] FIG. 9 is a schematic diagram of an exemplary configuration of a data driver according to the present invention;

[0031] FIG. 10 is a schematic diagram of an exemplary current sink data drive IC part of FIG. 9 according to the present invention;

[0032] FIG. 11 is a schematic circuit diagram of the current sink data drive IC part of FIG. 9 according to the present invention;

[0033] FIG. 12 is a schematic plan diagram of another exemplary active matrix-type electro-luminescence display device according to the present invention;

[0034] FIG. 13 is a schematic circuit diagram of an exemplary cell of an electro-luminescence display panel of FIG. 12 according to the present invention;

[0035] FIG. 14 is a schematic diagram of an exemplary configuration of a data driver according to the present invention;

[0036] FIG. 15 is a schematic diagram of an exemplary current sink data drive IC part of FIG. 14 according to the present invention;

[0037] FIG. 16 is a schematic circuit diagram of the current sink data drive IC part of FIG. 14 according to the present invention;

[0038] FIG. 17 is a schematic diagram of an exemplary configuration of a data driver according to the present invention;

[0039] FIG. 18 is a schematic diagram of an exemplary current source data drive IC part of FIG. 17 according to the present invention; and

[0040] FIG. 19 is a schematic circuit diagram of the current source data drive IC part of FIG. 17 according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0041] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0042] FIG. 4 is a schematic circuit diagram of an exemplary active matrix-type electro-luminescence display apparatus according to the present invention. In FIG. 4, an active matrix-type electro-luminescence display device may include an ELD panel 42 having a pixel 48 arranged at each intersection part of scan lines SL and data lines DL, a scan driver 44 to drive the scan lines SL, and a data driver 46 to drive the data lines DL. Each pixel 48 may be selected when scan pulses are supplied to the scan line SL of a cathode to generate light corresponding to a pixel signal, i.e., a current signal, supplied to the data line DL of an anode.

[0043] FIG. 5 is a schematic circuit diagram of an exemplary cell of an electro-luminescence display panel of FIG. 4 according to the present invention. In FIG. 5, each pixel 48 may include a cell driver 50 and an electro-luminescence (OEL) cell, wherein each OEL cell may be equivalently expressed as a diode connected between the data line DL and the scan line SL. Each OEL cell may emit light when a negative scan pulse is supplied to the scan line SL and, at the same time, a positive current is supplied to the data line DL in accordance with a data signal, thereby supplying a forward voltage. Conversely, a reverse voltage may be supplied to the OEL cell included in an unselected scan line, whereby no light is emitted. In other words, the light-emitting OEL cell may be charged with a forward charge, whereas the OEL cell with no light emission may be charged with a reverse charge.

[0044] The scan driver 44 may sequentially supply the negative scan pulse to scan lines SL by lines, and the data driver 46 may supplies a current signal to the data lines DL, wherein the current signal has a current level or pulse width corresponding to a data signal for each horizontal period. Accordingly, the ELD device may supply the current signal with the current level or pulse width proportional to input data to the OEL cell, wherein each OEL cell may emit light in proportion to the amount of current applied from the data line DL.

[0045] In FIG. 5, the cell driver 50 may include a first TFT T1 formed between a cell drive voltage source VDD and the OEL cell for driving the OEL cell, a second TFT T2 connected to the cell drive voltage source VDD to form a current mirror with the first TFT

T1, a third TFT T3 connected to the second TFT T2, the scan line SL, and the data DL for responding to a signal of the data line DL, a fourth TFT T4 connected to the gate terminals of the first TFT T1 and the second TFT T2, the scan line SL, and the third TFT T3, and a capacitor Cst connected between the cell drive voltage source VDD and the gate terminals of the first TFT T1 and the second TFT T2. For example, the first to fourth TFT T1 to T4 may include p-type MOSFETs.

[0046] The third and fourth TFT's T3 and T4 may be turned ON in response to a negative scan voltage from the scan line SL, whereby a current path may be enabled to conduct current between the source terminal and the drain terminal. In addition, the third and fourth TFT's T3 and T4 may remain at an OFF state when a voltage in the scan line SL is below the threshold voltage Vth of the third and fourth TFT's T3 and T4. A data voltage Vcl from the data line DL may be supplied to the gate terminal of the first TFT T1 through the third and fourth TFT's T3 and T4 during an ON period of time of the third and fourth TFT's T3 and T4. Conversely, each of the first and second TFT's T1 and T2 may remain open for the data voltage Vcl not to be supplied to the first TFT T1 during an OFF period of time of the first and second TFT's T1 and T2.

[0047] The first TFT T1 may control the current between the source terminal and the drain terminal by the data voltage Vcl supplied to the gate terminal of itself, wherein the OEL cell is made to emit light with a brightness corresponding to the data voltage Vcl. The

second TFT T2 may be configured to form a current mirror with the first TFT T1, thereby uniformly controlling current at the first TFT T1.

[0048] The capacitor Cst may store a voltage difference between the data voltage Vcl and a cell drive voltage VDD to uniformly sustain the voltage supplied to the gate terminal of the first TFT T1 for one frame period, and to uniformly sustain the current supplied to the OEL cell for one frame period. In addition, the data driver 46 controlling the pulse width of the current signal in response to the input data may include a plurality of data drive integrated circuits (ICs).

[0049] FIG. 6 is a schematic diagram of an exemplary configuration of a data driver according to the present invention, FIG. 7 is a schematic diagram of an exemplary current sink data drive IC part of FIG. 6 according to the present invention, and FIG. 8 is a schematic circuit diagram of the current sink data drive IC part of FIG. 6 according to the present invention. In FIGs. 6 to 8, a data driver 46 may include a plurality of current sink data drive IC's 52a, 52b, 52c, ..., which may be interconnected in a cascade circuit configuration. Each of the current sink data drive IC's 52a, 52b, 52c, ... may include a reference current supply/path part 54a and a current sink data drive IC 54b that may be driven by a reference current from the reference current supply/path part 54a.

[0050] In FIG. 7, the reference current supply/path part 54a may receive a reference constant current Iref generated from an exterior voltage source to supply the received current to the current sink data drive IC 54b. In addition, the reference current supply/path

part 54a may supply the same reference constant current (i) to an adjacent current sink data drive IC part 52b.

[0051] In FIG. 8, the reference current supply/path part 54a may include a first switching device D1 connected between a first voltage source VDD1 and a ground voltage source GND, second and third switching devices D2 and D3 connected to the ground voltage source GND to form a current mirror circuit with the first switching device D1, a fourth switching device D4 connected between the second switching device D2 and a second voltage source VDD2, and a fifth switching device D5 connected to the second voltage source VDD2 to form a current mirror circuit with the fourth switching device D4 and to transmit a reference current to the current sink data drive IC part 52b. In addition, the third switching device D3 may be included within the current sink data drive IC 54b. The first to third switching devices D1 to D3 may include n-type MOSFETs, and the fourth and fifth switching devices D4 and D5 may include p-type MOSFETs.

[0052] During operation, a reference current Iref may flow in the first switching device D1 in accordance with a current source using a first voltage source VDD1, and the same reference current Iref may flow in the second switching device D2 forming the current mirror with the first switching device D1. A current may flow in the fourth switching device D4 connected to the second voltage source VDD2 and the second switching device D2 as much as the reference current Iref flows through the second switching device D2. Accordingly, the same reference current Iref may flow in the fifth switching device D5

forming the current mirror with the fourth switching device D4, and the current may be supplied to the adjacent current sink data drive IC part 52b. Accordingly, the same current may be supplied to all current sink data drive IC's 54b within the data driver 46.

[0053] In FIG. 8, the current sink data drive IC 54b may include a reference MOSFET M0 connected between a third voltage source VDD3 and the third switching device D3, and constant current sources, i.e., constant current supply MOSFETs M1 to M4, connected in parallel to the reference MOSFET M0 with the voltage source VDD to form a current mirror circuit for supplying a constant current (i) to each data line connected to the OEL cell. Furthermore, the current sink data drive IC 54b may include switch devices S1 to S4 that are connected between each of the constant current supply MOSFETs M1 to M4 and the data line to control the supply time of the constant current (i) from the constant current supply MOSFET M1 to M4 in response to input data, thereby controlling the pulse width of the current signal. Accordingly, it may be possible for the current sink data drive IC 54b not to include the switch devices S1 to S4.

[0054] Each of the constant current supply MOSFETs M1 to M4 together with the reference MOSFET M0 receiving the supply voltage of the ground voltage source GND in parallel may form a current mirror circuit with the reference MOSFET M0, so the same amount of constant current (i) or 2^n times the constant current, i.e., 2i, 4i, 8i,..., may be supplied. The constant current (i) supplied from the constant current supply MOSFETs M1 to M4 may change in accordance with the amount of load, i.e., line resistance, of the

data lines and a capacitance that is related to the amount of light emission of the OEL cell due to the structure of the ELD panel. Accordingly, the current sink data drive IC 54b forming a current mirror circuit may include a plurality of current control resistors with a resistance value different from each other in order to control the changing current in accordance with the amount of load. In addition, a resistor may be selected among the plurality of current control resistors in accordance with an average amount of load of the current sink data drive IC 54b to be connected between the reference MOSFET M0 and the ground, thereby controlling the constant current (i) of the current sink data drive IC 54b.

[0055] FIG. 9 is a schematic diagram of an exemplary configuration of a data driver according to the present invention, FIG. 10 is a schematic diagram of an exemplary current sink data drive IC part of FIG. 9 according to the present invention, and FIG. 11 is a schematic circuit diagram of the current sink data drive IC part of FIG. 9 according to the present invention. In FIGs. 9 to 11, a data driver 46 may include a plurality of current sink data drive IC's 56a, 56b, 56c, ..., which may be interconnected in a cascade circuit configuration. Each of the current sink data drive IC's 56a, 56b, 56c, ... may include a reference current supply/path part 58a and a current sink data drive IC 58b that may be driven by a reference current from the reference current supply/path part 58a, as shown in FIG. 10.

[0056] In FIG. 10, the reference current supply/path part 58a may receive the reference constant current Iref generated from a ground voltage source to supply the received current

to the current sink data drive IC 58b. In addition, the reference current supply/path part 58a may supply the same reference constant current (i) to an adjacent current sink data drive IC part 56b.

[0057] In FIG. 11, the reference current supply/path part 58a may include a first switching device D1 connected between a first voltage source VDD1 and a ground voltage source GND, a second switching device D2 connected to the first voltage source VDD1 to form a current mirror circuit with the first switching device D1, a third switching device D3 connected between the second switching device and the ground voltage source GND, a fourth switching device D4 connected to the ground voltage source GND to form a current mirror circuit with the third switching device D3 and to transmit the reference current to the adjacent current sink data drive IC part 56b, and a fifth switching device D5 connected to the ground voltage source GND to form a current mirror circuit with the third switching device D3 and to supply the reference current to the current sink data drive IC part 58b. Accordingly, the fifth switching device D5 may be included within the current sink data drive IC 58b. The first and second switching devices D1 and D2 may include p-type MOSFETs, and the third to fifth switching devices D3 to D5 may include n-type MOSFETs.

[0058] During operation, a reference current Iref may flow through the source-drain terminals of the first switching device D1 in accordance with a pulse width of a current signal using the ground voltage source GND, and the same reference current Iref may flow

in the second switching device D2 forming the current mirror with the first switching device D1. The reference current Iref via the second switching device D2 may control the gate terminal of the third switching device D3, thereby causing the same reference current Iref to flow in the third switching device D3. Accordingly, the same reference current Iref may flow in the fourth switching device D4 that forms the current mirror circuit with the third switching device D3, and the same reference current Iref may also flow in the adjacent current sink data drive IC 56b connected to the fourth switching device D4. The fifth switching device D5 forming the current mirror circuit with the third switching device D3 may supply the reference current Iref into the current sink data drive IC 58b in the same manner as the third switching device D3. Accordingly, the same current may be supplied to all current sink data drive IC's 58b within the data driver 46.

[0059] The current sink data drive IC 58b may include a reference MOSFET M0 connected between a second voltage source VDD2 and the fifth switching device D5, and constant current sources, i.e., constant current supply MOSFETs M1 to M4, connected in parallel to the reference MOSFET M0 with the voltage source VDD to form a current mirror circuit for supplying a constant current (i) to each data line connected to the OEL cell. Furthermore, the current sink data drive IC 58b may include switch devices S1 to S4 that are connected between each of the constant current supply MOSFETs M1 to M4 and the data line to control a supply time of the constant current (i) from the constant current supply MOSFET M1 to M4 in response to input data, thereby controlling the pulse width

of the current signal. Accordingly, it may be possible for the current sink data drive IC 58b not to include the switch devices S1 to S4.

[0060] Each of the constant current supply MOSFETs M1 to M4 together with the reference MOSFET M0 receiving the supply voltage of the ground voltage source GND in parallel may form a current mirror circuit with the reference MOSFET M0, so the same amount of constant current (i) or 2^n times the constant current, i.e., 2i, 4i, 8i,..., may be supplied. The constant current (i) supplied from the constant current supply MOSFETs M1 to M4 may change in accordance with the amount of load, i.e., line resistance, of the data lines and a capacitance that is related to the amount of light emission of the OEL cell due to the structure of the ELD panel. Accordingly, the current sink data drive IC 58b forming a current mirror circuit may include a plurality of current control resistors with a resistance value different from each other in order to control the changing current in accordance with the amount of load. In addition, a resistor may be selected among the plurality of current control resistors in accordance with an average amount of load of the current sink data drive IC 58b to be connected between the reference MOSFET M0 and the ground, thereby controlling the constant current (i) of the constant current data drive IC 58b.

[0061] FIG. 12 is a schematic plan diagram of another exemplary active matrix-type electro-luminescence display device according to the present invention. In FIG. 12, an active matrix-type ELD device may include an ELD panel 62 having a pixel 68 arranged at

each intersection part of scan lines SL and data lines DL, a scan driver 64 to drive the scan lines SL, and a data driver 66 to drive the data lines DL.

[0062] FIG. 13 is a schematic circuit diagram of an exemplary cell of an electro-luminescence display panel of FIG. 12 according to the present invention. In FIG. 13, each pixel may be selected when scan pulses are supplied to the scan line SL of a cathode to generate light corresponding to a pixel signal, i.e., a current signal, supplied to the data line DL of an anode. In addition, each pixel may include a cell driver 70 and an OEL cell, wherein the OEL cell may be equivalently expressed as a diode connected between the data line DL and the scan line SL. Each OEL cell may emit light when a negative scan pulse is supplied to the scan line SL and, at the same time, a positive current is supplied to the data line DL in accordance with a data signal, thereby supplying a forward voltage. Conversely, a reverse voltage may be supplied to the OEL cell included in an unselected scan line, whereby no light may be emitted. In other words, the light-emitting OEL cell may be charged with a forward charge, whereas the OEL cell with no light emission may be charged with a reverse charge.

[0063] The scan driver 64 may sequentially supply the negative scan pulse to scan lines SL by lines, and the data driver 66 may supply a current signal to the data lines DL, wherein the current signal may have a current level or pulse width corresponding to a data signal for each horizontal period. Accordingly, the ELD device may supply the current signal with the current level or pulse width proportional to input data to the OEL cell. In

addition, each OEL cell may emit light in proportion to the amount of current applied from the data line DL.

[0064] In FIG. 13, the cell driver 70 may include a first TFT T1 formed between a ground voltage source GND and the OEL cell for driving the OEL cell, a second TFT T2 connected to the ground voltage source GND to form a current mirror with the first TFT T1, a third TFT T3 connected to the second TFT T2, the scan line SL, and the data DL for responding to a signal of the data line DL, a fourth TFT T4 connected to the gate terminals of the first TFT T1 and the second TFT T2, the scan line SL, and the third TFT T3, and a capacitor Cst connected between the ground voltage source GND and the gate terminals of the first TFT T1 and the second TFT T2. The first to fourth TFT T1 to T4 may include n-type MOSFETs.

[0065] The third and fourth TFT's T3 and T4 may be turned ON in response to a positive scan voltage from the scan line SL, thus a current path may be enabled to conduct current between the source terminal and the drain terminal of the third and fourth TFT's T3 and T4. In addition, the third and fourth TFT's T3 and T4 may remain at an OFF state when a voltage in the scan line SL is below the threshold voltage Vth of the third and fourth TFT's T3 and T4. A data voltage from the data line DL may be supplied to the gate terminal of the first TFT T1 through the third and fourth TFT's T3 and T4 during an ON period of time period of the third and fourth TFT's T3 and T4. Conversely, each of the first and

second TFT's T1 and T2 may be open for the data voltage Vcl not to be supplied to the first TFT T1 during an OFF period of time of the first and second TFT's T1 and T2.

[0066] The first TFT T1 may control the current between the source terminal and the drain terminal by the data voltage Vcl supplied to the gate terminal of the first TFT T1, whereby the OEL cell may be made to emit light with a brightness corresponding to the data voltage Vcl by way of a voltage difference between the ground voltage source GND and the cell drive voltage source VDD. The second TFT T2 may be configured to form a current mirror with the first TFT T1, thereby uniformly controlling current at the first TFT T1.

[0067] The capacitor Cst may store a voltage difference between the data voltage Vcl and the ground voltage source GND to uniformly sustain the voltage supplied to the gate terminal of the first TFT T1 for one frame period, and to uniformly sustain the current supplied to the OEL cell for one frame period. Accordingly, the data driver 66 controlling the pulse width of the current signal in response to the input data may include a plurality of data drive IC's.

[0068] FIG. 14 is a schematic diagram of an exemplary configuration of a data driver according to the present invention, FIG. 15 is a schematic diagram of an exemplary current sink data drive IC part of FIG. 14 according to the present invention, and FIG. 16 is a schematic circuit diagram of the current sink data drive IC part of FIG. 14 according to the present invention. In FIGs. 14 to 16, a data driver 66 may include a plurality of current source data drive IC's 72a, 72b, 72c, ..., which may be interconnected in a cascade circuit

configuration. Each of the current source data drive IC's 72a, 72b, 72c, ... may include a reference current supply/path part 74a and a current source data drive IC 74b that may be driven by a reference current from the reference current supply/path part 74a, as shown in FIG. 15.

[0069] In FIG. 15, the reference current supply/path part 74a may receive the reference constant current Iref generated from an exterior voltage source to supply the received current to the current source data drive IC 74b. In addition, the reference current supply/path part 74a may supply the same reference constant current (i) to an adjacent current source data drive IC part 72b.

[0070] In FIG. 16, the reference current supply/path part 74a may include a first switching device D1 connected between a first voltage source VDD1 and a ground voltage source GND, second and third switching devices D2 and D3 connected to the ground voltage source GND to form a current mirror circuit with the first switching device D1, a fourth switching device D4 connected between the second switching device D2 and a second voltage source VDD2, and a fifth switching device D5 connected to the second voltage source VDD2 to form a current mirror circuit with the fourth switching device D4 and to transmit a reference current to the current source data drive IC part 72b. Accordingly, the third switching device D3 may be included within the current source data drive IC 74b. The first to third switching devices D1 to D3 may include n-type MOSFETs, and the fourth and fifth switching devices D4 and D5 may include p-type MOSFETs.

[0071] During operation, a reference current Iref may flow in the first switching device D1 in accordance with a current source using a first voltage source VDD1, and the same reference current Iref may flow in the second switching device D2 forming the current mirror with the first switching device D1. A current may flow in the fourth switching device D4 connected to the second voltage source VDD2 and the second switching device D2 as much as the reference current Iref may flow through the second switching device D2. The same reference current Iref may flow in the fifth switching device D5 forming the current mirror with the fourth switching device D4, and the current may be supplied to the adjacent current source data drive IC part 72b. Accordingly, the same current may be supplied to all current source data drive IC's 74b within the data driver 66.

[0072] The current source data drive IC 74b may include a reference MOSFET M0 connected between a third voltage source VDD3 and the third switching device D3, and constant current sources, i.e., constant current supply MOSFETs M1 to M4, connected in parallel to the reference MOSFET M0 with the third voltage source VDD3 to form a current mirror circuit for supplying a constant current (i) to each data line connected to the OEL cell. Furthermore, the current source data drive IC 74b may include switch devices S1 to S4 that may be connected between each of the constant current supply MOSFETs M1 to M4 and the data line to control a supply time of the constant current (i) from the constant current supply MOSFET M1 to M4 in response to input data, thereby controlling

the pulse width of the current signal. Accordingly, it may be possible for the current source data drive IC 74b not to include the switch devices S1 to S4.

[0073] Each of the constant current supply MOSFETs M1 to M4 together with the reference MOSFET M0 receiving the supply voltage of the third voltage source VDD3 in parallel may form a current mirror circuit with the reference MOSFET M0, so the same amount of constant current (i) or 2^n times the constant current, i.e., 2i, 4i, 8i,..., may be supplied. The constant current (i) supplied from the constant current supply MOSFETs M1 to M4 may change in accordance with the amount of load, i.e., line resistance, of the data lines and a capacitance that is related to the amount of light emission of the OEL cell due to the structure of the ELD panel. Accordingly, the current source data drive IC 74b forming a current mirror circuit may include a plurality of current control resistors with a resistance value different from each other at an exterior thereof in order to control the changing current in accordance with the amount of load. In addition, a resistor may be selected among the plurality of current control resistors in accordance with an average amount of load of the current source data drive IC 74b to be connected between the reference MOSFET M0 and the ground, thereby controlling the constant current (i) of the current source data drive IC 74b.

[0074] FIG. 17 is a schematic diagram of an exemplary configuration of a data driver according to the present invention, FIG. 18 is a schematic diagram of an exemplary current source data drive IC part of FIG. 17 according to the present invention, and FIG. 19 is a

schematic circuit diagram of the current source data drive IC part of FIG. 17 according to the present invention. In FIGs. 17 to 19, a data driver 66 may include a plurality of current source data drive IC's 76a, 76b, 76c, ..., which may be interconnected in a cascade circuit configuration. Each of the current source data drive IC's 76a, 76b, 76c, ... may include a reference current supply/path part 78a and a current source data drive IC 78b that may be driven by a reference current from the reference current supply/path part 78a, as shown in FIG. 18.

[0075] In FIG. 18, the reference current supply/path part 78a may receive the reference constant current Iref generated from the ground voltage source GND to supply the received current to the current source data drive IC 78b and may supply the same reference constant current (i) to an adjacent current source data drive IC part 76b.

[0076] In FIG. 19, the reference current supply/path part 78a may include a first switching device D1 connected between a first voltage source VDD1 and a ground voltage source GND, a second switching device D2 connected to the first voltage source VDD1 to form a current mirror circuit with the first switching device D1, a third switching device D3 connected between the second switching device D2 and the ground voltage source GND, a fourth switching device D4 connected to the ground voltage source GND to form a current mirror circuit with the third switching device D3 and to transmit the reference current to the adjacent current source data drive IC part 76B, and a fifth switching device D5 connected to the ground voltage source GND to form a current mirror circuit with the third

switching device D3 and to supply the reference current to the current source data drive IC part 78b. Accordingly, the fifth switching device D5 may be included within the current source data drive IC 78b. The first and second switching devices D1 and D2 may include p-type MOSFETs, and the third to fifth switching devices D3 to D5 may include n-type MOSFETs.

[0077] During operation, a reference current Iref may flow through the source-drain terminals of the first switching device D1 in accordance with the pulse width of a current signal using the ground voltage source GND, and the same reference current Iref may flow in the second switching device D2 forming the current mirror with the first switching device D1. The reference current Iref via the second switching device D2 may control the gate terminal of the third switching device D3, thereby causing the same reference current Iref to flow in the third switching device D3. Accordingly, the same reference current Iref may flow in the fourth switching device D4 that forms the current mirror circuit with the third switching device D3, and the same reference current Iref may also flow in the adjacent current source data drive IC 76b connected to the fourth switching device D4. The fifth switching device D5 forming the current mirror circuit with the third switching device D3 may supply the reference current Iref into the current source data drive IC 78b in the same manner as the third switching device D3. Accordingly, the same current may be supplied to all current source data drive IC's 78b within the data driver 66.

[0078] In FIG. 19, the current source data drive IC 78b may include a reference MOSFET M0 connected between a second voltage source VDD2 and the fifth switching device D5, and constant current sources, i.e., constant current supply MOSFETs M1 to M4, connected in parallel to the reference MOSFET M0 with the second voltage source VDD2 to form a current mirror circuit for supplying a constant current (i) to each data line connected to the OEL cell. Furthermore, the current source data drive IC 78b may include switch devices S1 to S4 that may be connected between each of the constant current supply MOSFETs M1 to M4 and the data line to control a supply time of the constant current (i) from the constant current supply MOSFET M1 to M4 in response to input data, thereby controlling the pulse width of the current signal. Accordingly, it may be possible for the current source data drive IC 78b not to include the switch devices S1 to S4.

[0079] Each of the constant current supply MOSFETs M1 to M4 together with the reference MOSFET M0 receiving the supply voltage of the second voltage source VDD2 in parallel may form a current mirror circuit with the reference MOSFET M0, so the same amount of constant current (i) or 2^n times the constant current, i.e., 2i, 4i, 8i,..., may be supplied. The constant current (i) supplied from the constant current supply MOSFETs M1 to M4 may change in accordance with the amount of load, i.e., the line resistance, of the data lines and a capacitance that is related to the amount of light emission of the OEL cell due to the structure of the ELD panel. Accordingly, the current source data drive IC 78b forming a current mirror circuit may include a plurality of current control resistors

with a resistance value different from each other at an exterior thereof in order to control the changing current in accordance with the amount of load. In addition, a resistor may be selected among the plurality of current control resistors in accordance with an average amount of load of the current source data drive IC 78b to be connected between the reference MOSFET M0 and the ground, thereby controlling the constant current (i) of the constant current data drive IC 78b.

[0080] It will be apparent to those skilled in the art that various modifications and variations can be made in the method and apparatus for data-driving an electro-luminescence display panel device of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.